SOPC implementation for stereovision measurement system

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ABSTRACT

Image processing is necessary for three-dimensional information recovering of stereovision measurement system and it is always bottleneck for real-time applications. In order to accelerate system computational power, the design of SOPC system which can fulfills image processing tasks parallel is discussed. As a part of high-speed stereovision measurement system, the application specific SOPC is designed as an embedded PCI board card of hosts PC. This paper focuses on three aspects. Firstly, Principles of SOPC system designing and SOPC features selecting are analyzed with measuring requirements under consideration. Then the realization of SOPC system is described in detail. The embedded processor, special IPs (Intelligent Properties), several custom logic modules are included in a single FPGA. All units are seamlessly integrated into the overall system using the system builder interface. The parallel processing is illustrated by examples. In the end, simulation and debugging results of SOPC system are introduced. Elements that influence running time are analyzed and final results are given. Experiment and test results show that all the functions needed were realized with much higher efficiency and processing speed in our SOPC system than conventional software.

Keywords: vision measurement, image processing, FPGA, SOPC, Avalon bus, processing speed

1. INTRODUCTION

Machine vision technology has become a viable target in the fields of reverse engineering and industrial products qualify inspection. In stereovision measurement systems, image capturing, image processing, point matching or registration, camera calibrating, 3-D coordinate transferring and 3-D reconstructing are the key steps to recover three-dimensional information of a scene. According to traditional implementation method, after images are captured by CCD (Charge Coupled Device) or CMOS (Complementary Metal-Oxide-Semiconductor) cameras, a large number of images are transferred to the computer and the specific software fulfills all the data processing steps.

Data processing of stereovision measurement systems typically requires very high computational power, and it is always bottleneck for real-time system. From this point of view, the traditional software method has become less useful in high speed processing realm, and the parallel processing capabilities of hardware are attractive implementation options for those highly repetitive tasks. From the available literature, some hardware methods that are used to accelerate system computational power can be searched, such as multiple DSPs (Digital Signal Processors), or DSP+FPGA, or special parallel processors etc. Different with above schemes, a single FPGA (Field Programmable Gate Arrays) with an embedded processor and DSP module is used to construct a SOPC (System On a Programmable Chip) system that fulfills part of data processing tasks parallel, this can deliver the requisite level of computing power more cost-effectively and simplify hardware complexity. The design of such system is discussed in this paper.

2. ARCHITECTURE OF STEREOVISION SYSTEM USING SOPC TECHNOLOGY

The application specific SOPC system is designed for 3-D close-range photogrammetry system. It is constructed as an embedded PCI (Peripherals Component Interconnect) board card of host PC (Personal Computer). There are large storage memory chips, the PCI bridge, the FPGA chips, and other control circuits on this board. This embedded PCI board is used as sub-system of measurement system.

2.1 Principles of SOPC system designing

Computational tasks of stereovision measurement system are divided into three types according to input data quantity

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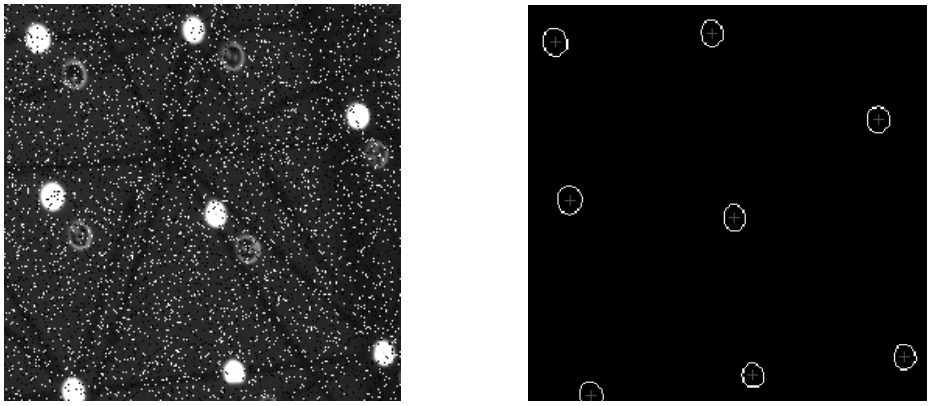
and algorithm complicity. Tasks with little data input flow and complicated algorithm, such as camera calibration and image matching etc., are fulfilled by software of host PC. The other two type tasks with simple algorithm and large or little input data flow, such as image pre-processing and the coordinates obtaining of target points, are executed by the SOPC system. With system requirements under consideration, features of SOPC system are selected.

The input of SOPC system is gray image that captured by the image sensors and saved as bit-map files. The output of SOPC system is two-dimensional coordinates of all the target points that are detected from original images. They are showed in figure 1.



a. Input of SOPC system (part) b. Output of SOPC system (part)

Fig. 1. Input and output of SOPC system

In order to build SOPC system, EP1S40 (belongs to Stratix series), one kind of FPGA chip of Altera company (Stratix series), in which NIOS soft processor and DSP modules are included, is selected as core chip.

2.2 System overview

The hardware construction of the stereovision measurement system with SOPC system is described as figure 2.

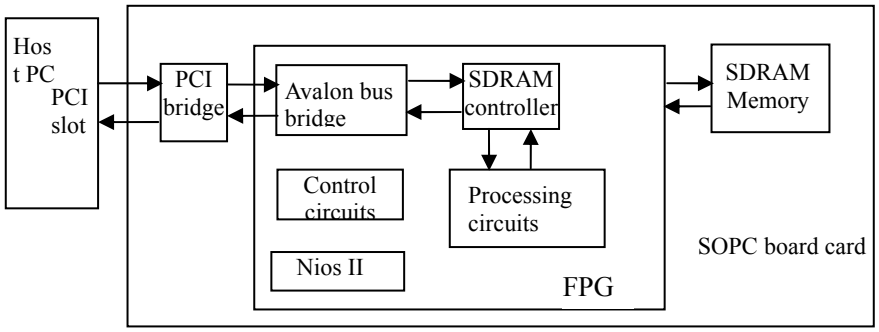


Fig. 2. Hardware construction of stereovision measurement system using SOPC technology

From the view of stereovision measurement system, there are two kinds of data processing tasks: One is finished by microprocessor of host PC, and the other is executed by SOPC based on FPGA. When system is running, image data are transferred between host PC and SOPC system. Data exchanging speed must meet the requirements of SOPC system data rate. PCI bus is selected as communicating channel. When embedded PCI board card are designed, several factors should be considered:

a. Bridge between PCI bus and build-in bus of FPGA chip.

b. Large memory is needed to store input image data and output result in SOPC system. Memory units that can be used in FPGA chip are very limited. So external memory chips must be applied. High-speed SDRAM (Synchronous Dynamic Random Access Memory) is a good choice.

c. If SDRAM chips are selected to be data buffer, DMA (Direct Memory Access) or other high-speed data transferring method should be applied. So DMA controller and SDRAM controller must be developed.

2.3 Processing analyze of stereovision measurement system

Flow chart of measurement system is illustrated as figure 3.

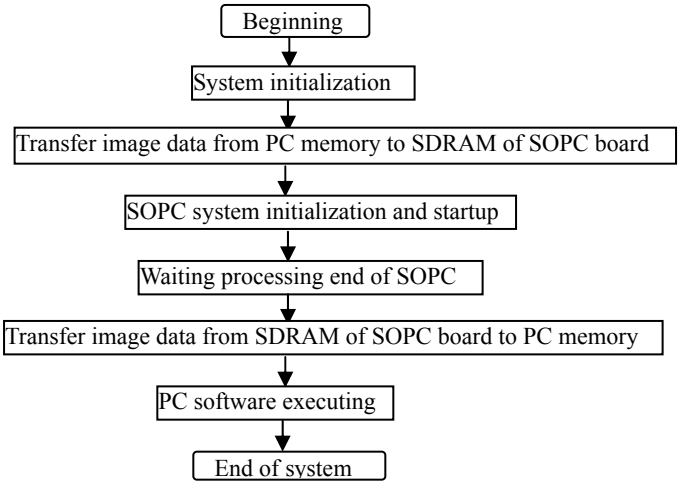


Fig. 3. Flow chart of stereovision measurement system using SOPC technology

3. IMPLEMENTATION OF SOPC SYSTEM

The hardware construction of the embedded PCI board card is showed in figure 4.

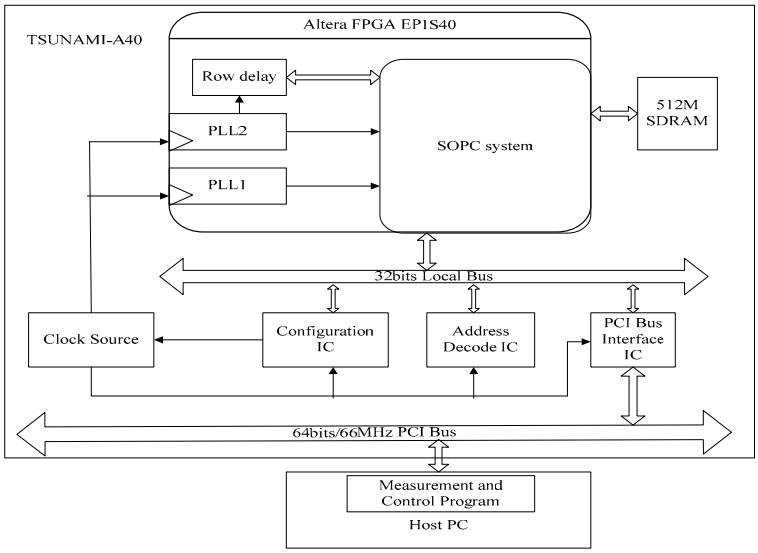


Fig. 4. Overall hardware structure of the PCI board card embedded in host PC

3.1 Design of SOPC system

As showed in figure 4, SOPC system is built inside a single FPGA chip (Altera EP1S40). The input and output data of SOPC system are described in chapter 2.1: gray image and two-dimensional coordinates of all the target points. The following factors should be considered:

a. How to transfer data between outside SDRAM and inside buffers?

b. How to produce image frame synchronization signal and use this signal to synchronize the parallel modules?

c. Several IPs (intellectual property) are used or built to fulfill special functions. Application specific program is run by NIOS soft microprocessor. They aren't independent. Using Avalon bus to control and manage data exchange between different modules is important and difficult.

d. Data exchange between Avalon bus and PCI local bus.

e. The debug methods of IPs and NIOS program.

f. Clock signals generation.

The hardware structure of SOPC system is illustrated by figure 5. Interrupt controller, image pre-processing module, memory controller, SDRAM controller, NIOS and other modules are designed as host device or slave devices of Avalon bus. Their requirements for bus usage are arbitrated and delivered by Avalon bus controller.

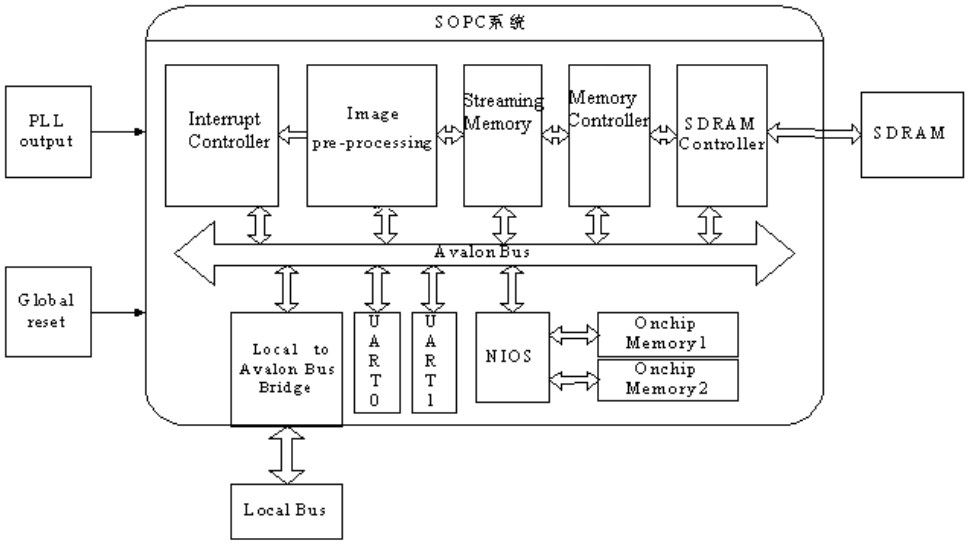


Fig. 5. Hardware structure of SOPC system built in single chip FPGA (Altera EP1S40)

After image data are transferred into SDRAM and SOPC system is reset and reconfigured by control program of host PC, image pre-processing modules and NIOS work independently, but they need to share some information. For example, result of one step image pre-processing is input signal of NIOS program, and vice versa. Interrupt mechanism is used for these situations. Some output signals of image pre-processing module are linked to interrupt controller.

The memory spaces of NIOS are located in different devices. The boot program is located at on-chip memory of NIOS. Data memory and program memory of NIOS are independent each other. They are located outside NIOS: on-chip memory 1 and on-chip memory 2 of FPGA chip.

There are two UART (Universal Asynchronous Receiver/Transmitter) serial port devices linked to Avalon bus. One is used to download the NIOS program to on-chip memory of FPGA, and the other is used to debug NIOS program.

The data exchange of SOPC system and host PC is accomplished through PLX9656 chip. This is bridge between Avalon bus and PCI local bus.

3.2 Analyze of image pre-processing module and NIOS

As described in chapter 2.1, the input of SOPC system is gray image, and the output is two-dimensional coordinates of the target points. The following steps should be done to detect all the target points from original images and calculate two-dimensional coordinates of those points: median filtering, histogram generating, threshold calculating, image binarizing, edge detecting, point center calculating and etc. All these functions are achieved by different sub-modules of

image pre-processing module and NIOS program. In order to accelerate the stereovision measurement system, all the above functions should to run parallel. But this is impossible. For example, threshold calculating module must start after the end of histogram generating module. But histogram generating module can start after median filtering generates one row. From this point of view, the acting sequence of all the functional modules is mixture of parallel mode and serial mode.

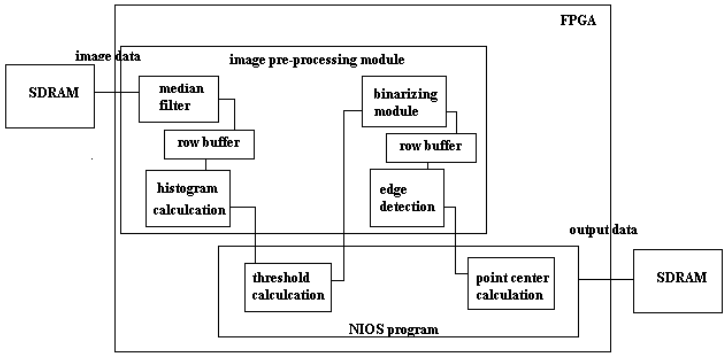


Fig. 6. Relationship between sub-modules of image pre-processing module and NIOS program

As showed in figure 6, median filtering, histogram generating, image binarizing, and edge detecting are realized by sub-modules of image pre-processing module. Median filtering and histogram generating are designed to work parallel; there is a row buffer to help their data transferring. The relationship of image binarizing and edge detecting is the same.

Histogram generating, threshold calculating, edge detecting and point center calculating modules act serially. After histogram generating finished, it generates an interrupt signal. NIOS processor starts threshold calculating function when it detects this interrupt signal. The relationship of edge detecting and point center calculating is the same.

Synchronous signals between different sub-modules are not illustrated in figure 6.

3.3 Realizing of sub-modules of image pre-processing

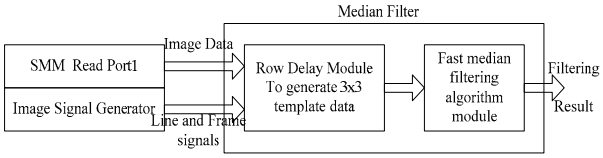


Fig. 7. Block diagram of median filtering sub-module

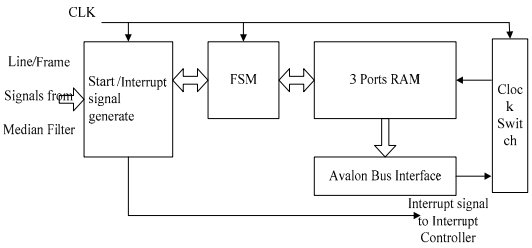


Fig. 8. Block diagram of histogram generating sub-module

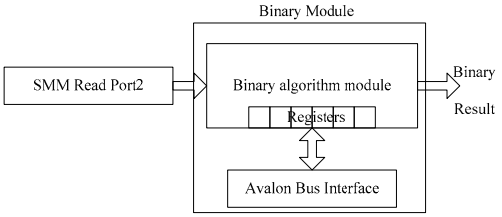


Fig. 9. Block diagram of binarizing sub-module

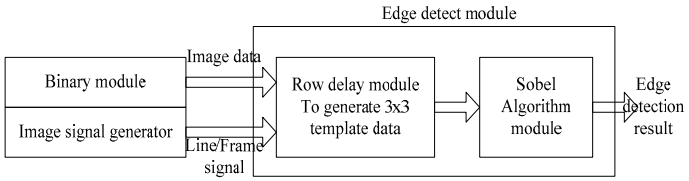


Fig. 10. Block diagram of edge detecting sub-module

The block diagrams of functional sub-modules described in chapter 3.2 are illustrated in figure 7-10. The detail technical discussions can be found in reference 6.

4. EXPERIMENTAL RESULTS AND CONCLUSIONS

The realization of SOPC system designing for 3-D close-range photogrammetry system is discussed in chapter 2 and 3. The embedded processor, special IPs (Intelligent Properties), several custom logic modules are included in a single FPGA. All units are seamlessly integrated into the overall system using the system builder interface. Different tasks are distributed to different units according to characteristics of processing algorithms. Data exchange between units of SOPC is fulfilled by inside bus. The parallel processing is illustrated by examples. Simulation and debugging results of SOPC system are presented in the figure 11-14.

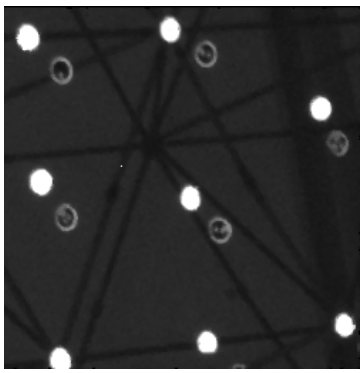


Fig. 11. Output of median filtering sub-module
(Input of median filtering is image data showed in figure 1a)

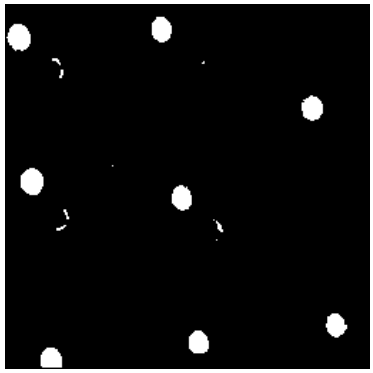


Fig. 12. Output of binarizing sub-module
(Input of binarizing is image data showed in figure 11)

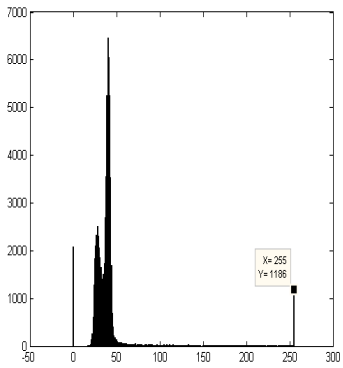


Fig. 13. Output of histogram generating sub-module
(Input of histogram generating is image data showed in figure 11)

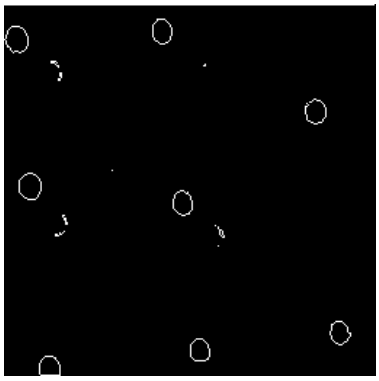


Fig. 14. Output of edge detecting sub-module
(Input of edge detecting is image data showed in figure 12)

Image data showed in figure 1a are the input of the SOPC system. The full image size is 3070*2048 pixels, and figure 1a is one part of the full image. The width of each pixel is 8 bits and gray level is 256. The frequency of SOPC input clock is 50MHz. Clock signals used by image pre-processing sub-modules and NIOS are different; they are generated by PLL circuits inside SOPC system.

In order to verify the functions of different image pre-processing sub-modules, some debug tools are used to download and upload semi-finished data to or from outside SDRAM or on-chip memory. Semi-finished data showed in figure 11-14 are the results of median filtering, binarizing, histogram generating and edge detecting. The final result (two-dimensional coordinates of all the target points that are detected from original images, calculated by NIOS) is showed in figure 1b.

Running time of SOPC system lies on the following factors: download time of transferring image data to SDRAM though PCI bus; running time of image pre-processing sub-modules; running time of NIOS program; upload time of transferring image data from SDRAM to host PC. Experimental result indicates that the actual speed can meet the requirement of measurement system.

The scheme of SOPC system discussed in the paper can be improved by changing data transferring mode and enhancing efficiency of NOIS processor. Data transferring is time-consuming operation. If image information captured by CCD or CMOS cameras are stored to SDRAM directly (not transferred through PCI bus of host PC), running time will be reduced greatly.

5. ACKNOWLEDGE

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